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EASY SIMULATION AND DESIGN OF ON-CHIP INDUCTORS IN STANDARD CMOS PROCESSES

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ABSTRACT

This paper presents an approach to CMOS inductor modelling, that allow easy simulation in SPICE-like simulators. A number of test results are presented concerning optimal center hole, inductor area, wire spacing and self-inductance. Finally a comprehensive design guide is provided on how to design close-to-optimal inductors without the use of electromagnetic simulators.

1. INTRODUCTION

On-Chip CMOS inductors have many desirable features for the use in RF applications. Unfortunately these inductors suffer from low Q-values due to high series resistance, substrate losses and other parasitics. Designers have failed to model all of these effects accurately enough to produce the optimal on-chip silicon inductor, or to present a design methodology that ensures the optimal inductor for a given application. 3-D Finite Element simulations are the best we can do in terms of predicting inductor behaviour, but they are slow and they do not guarantee that the optimal inductor is found as all possible solutions can not be simulated.

The purpose of this work has been to gain knowledge about the influence of the design parameters on the inductor quality, on the peak-Q frequency and on the self-inductance. Furthermore it has been a goal to develop a simple yet accurate inductor model and to make a good design guide. The paper will try to present results of this work. Section 2 describes the parasitics that affect the inductor quality. Section 3 treats the modelling aspects. Section 4 presents some measurements and test results. Section 5 contains a comprehensive design guide. Section 6 discusses multi-layer inductors and finally section 7 concludes the paper.

2. PARASITICS

On-chip inductors in CMOS processes are affected by the proximity of a low resistivity substrate. Typically the resistivity is in the order 0.01Ω·cm which is considerably lower than what is typically used in bipolar and BiCMOS processes. This means that eddy currents in the substrate have a greater impact on the inductor quality in CMOS processes that in other silicon processes.

A cross-section of a circular inductor is shown in figure 1. It shows how the magnetic flux generated by the inductor current, penetrate the substrate and the innermost inductor turns and thereby induce eddy currents.

There are three kinds of losses in CMOS inductors. The first is the series resistance of the inductor. At DC the series resistance is determined mainly by the sheet resistance and by the inductor length. At higher frequencies eddy currents, skin effect and Hall effect make the current-flow in the inductor turns non-uniform and thereby increase the effective series resistance.

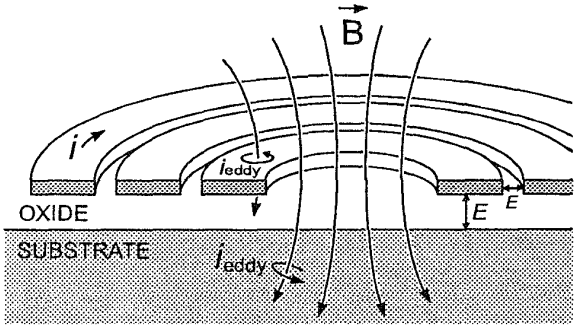

Figure 1. CMOS inductor physics.

The second source for losses is the capacitive coupling to the conducting substrate. This coupling makes the substrate potential immediately under the inductor turns vary which makes replacement currents flow in the substrate and thereby power is dissipated. The third contribution is the power that is dissipated due to eddy currents in the substrate and in the inner most inductor turns. Eddy currents increase with rising frequency therefore this contribution is also frequency dependent.

The capacitive effects do not directly reduce the quality of the inductor but they do reduce the effective inductance and above a certain frequency (the self-resonance frequency) they make the inductor useless as an inductor.

3. MODELLING

The behaviour of CMOS inductors can be modelled in a number of different ways [1]-[5]. We use the model shown in figure 2. It is composed of an ideal inductance L coupled in series with a frequency dependent resistor $R(f)$. The capacitive coupling to the semi-conducting substrate is modelled with a capacitance C_1 and C_2 from each port to two equal sized resistors R_{SUB}. Finally the capacitive coupling from port1 to port2 is modelled with C_{12}.

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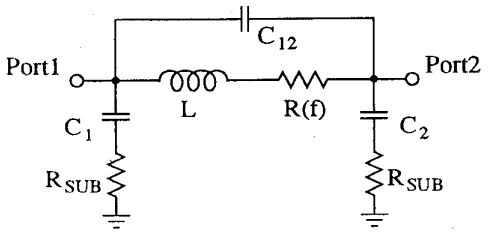

Figure 2. Freq. dep. lumped element inductor model.

The inductance L can be estimated by using CAE tools like EEsof, Momentum, APLAC or FastHenry. If the design rules presented in section 5 are applied, the following empirical formula can be used instead.

$$L \approx l \cdot (1.05 + 0.19 \cdot n) \quad nH \tag{1}$$

$$l \approx 1.027 \cdot \frac{\pi}{S+W} \cdot \left(R_O^2 - R_I^2\right) \tag{2}$$

Where l is the inductor length in mm and n is the number of turns. Formula (2) can be used to calculate the length of an octal inductor. S is the metal spacing and W is the wire width. R_O and R_I denote the distances from the center of the inductor to the middle of the outermost and innermost segments respectively.

The frequency dependent resistance $R(f)$ can be estimated using another empirical formula.

$$R(f) \approx R_0 + k_1 \cdot f^{k_2} \tag{3}$$

R_0, the DC resistance of the inductor is easily calculated as the sheet resistance multiplied by the ratio l/W. We found that $k_1 \approx 0.55\Omega$ and that $k_2 \approx 1.2$. The frequency f should be inserted in GHz.

The capacitances can be calculated using CAE tools, or empirical formulas [6] or by using the following simplified formulas.

$$C_{VA} \approx C_A \cdot (A_{IND} + A_{FRI} - A_{BRI}) \tag{4}$$

$$C_1 \approx C_{VA}/2 + C_{CON1} \tag{5}$$

$$C_2 \approx C_{VA}/2 + C_{BRI} + C_{CON2} \tag{6}$$

Here C_{AV} is the capacitance of a virtual inductor area seen from the substrate. C_A is the parallel plate-capacitance per area between the inductor layer and the substrate. A_{IND} is the area that the inductor covers (including the metal spacing). A_{FRI} is an area corresponding to the additional fringing contribution (approx. 3.5μm × total perimeter). A_{BRI} is the area of the bridge connecting the center of the inductor to the outside (port2). C_{CON1} and C_{CON2} are the capacitances of the inductor-connections. Finally C_{BRI} is the capacitance between the bridge and the substrate. C_{12} can be estimated using (7) where C_{IW} denote the inter-winding capacitance. C_{IW} is approximately 0.066fF/μm when a 2μm spacing and a single 1μm thick metal layer are used. Otherwise C_{IW} can be calculated using the empirical formula (8) [6]. T = thickness of metal, H = thickness of dielectric under conductor and ε = dielectric permittivity of the insulator. Note that l in (7) is the total length of spacing and that it can be calculated using (2).

$$C_{12} \approx l \frac{C_{IW}}{n-1} + \frac{C_{BRI2IND}}{2} \tag{7}$$

$$C_{IW} \approx 1.064 \cdot \varepsilon \cdot \left(\frac{T}{S}\right) \cdot \left(\frac{T+2H}{T+2H+0.5S}\right)^{0.695} + \varepsilon \cdot \left(\frac{W}{W+0.8S}\right)^{1.4148} \cdot \left(\frac{T+2H}{T+2H+0.5S}\right)^{0.804} + 0.831 \cdot \varepsilon \cdot \left(\frac{W}{W+0.8S}\right)^{0.055} \cdot \left(\frac{2H}{2H+0.5S}\right)^{3.542} \tag{8}$$

$$R_{SUB} \approx 50\,\Omega \tag{9}$$

$C_{BRI2IND}$ is the capacitance between the bridge and the inductor. The resistor R_{SUB} was found to be approximately 50 Ω in the used CMOS process (with a substrate resistivity of 0.01 Ω·cm).

4. EXPERIMENTAL MEASUREMENTS

A large number of different test inductors have been fabricated in a three metal layer 0.5 micron standard CMOS process. This section will present some of the results of the analysis of these inductors.

A large spacing gives a higher series resistance (as W must be reduced). On the other hand a too small spacing gives a high capacitive coupling and thus a lower frequency of operation. Five inductors with the spacing swept from 1.2μm to 4.0μm (1.2μm, 1.5μm, 2.0μm, 2.8μm & 4.0μm) were integrated in order to investigate what the optimal spacing is. The metal pitch (S+W) was kept constant at 8 μm and all other parameters were left unchanged. S-parameter measurements were performed and the data was converted into Y-parameters. Then the pad parasitics were de-embedded and the Q-values were calculated using the classic Q-value definition (10).

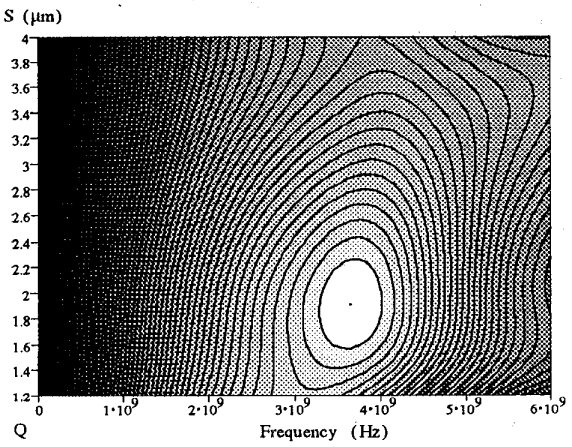

Figure 3. Measured Q-surface. Metal spacing vs. frequency.

$$Q_1 \approx \frac{-\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \qquad (10)$$

The resulting Q-curves were smoothed using a loess smoothing function and placed in a matrix. Finally a Q-surface was generated by applying curve fitting in the spacing-domain. The resulting contour plot is shown in figure 3.

As expected we see an optimum close to two micron. The peak (Q = 4.3) is found at a spacing of 1.9μm. It can also be observed that the capacitive coupling reduces the peak-Q frequency considerably below 1.5μm. Above 2.2 μm we can see a steady reduction of the quality factor corresponding to the increased series resistance.

The wire length, the number of turns and the size of the center hole are the parameters that have the greatest effect on the self-inductance of an inductor. In figure 4 the *L/l* ratios of 21 different inductors (large, small, square, octal, large center hole and small center hole) are shown against the number of inductor turns.

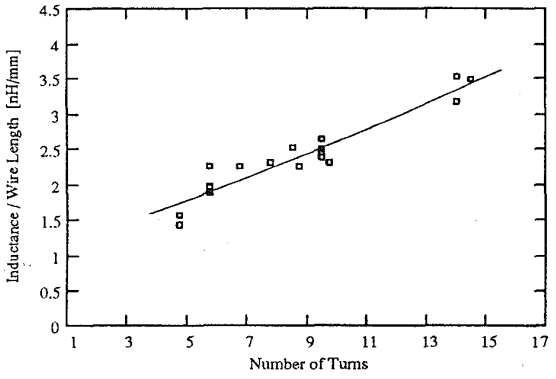

Figure 4. Inductance-length ratio vs. inductor turns.

The line is a second order polynomial regression that shows the average relation. It is interesting to note that the measurements below the line generally are inductors with small center holes and the ones above the line are inductors with large center holes. This confirms the theory that energy is lost due to negative coupling and eddy currents in the innermost turns when the center hole is too small. Using the design rules from section 5, these results lead to the empirical formula (1).

The peak-Q frequency is determined mainly by the capacitance to the substrate and the (frequency dependent) inductive losses in the substrate. Both effects increase with a growing inductor area (the latter because the flux must travel longer). This means, that the inductor area determines the peak-Q frequency. Figure 5 shows a plot of the peak-Q frequency versus the inverse virtual inductor area for a number of very different inductors (large, small, square, octal,..). The virtual inductor area is an area corresponding to the inductor with fringing fields. The line is a second order polynomial regression. Below 3 GHz we find that a linear approximation has a sufficient accuracy.

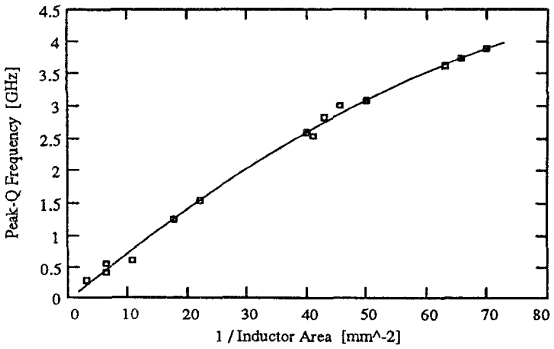

Figure 5. Peak-Q frequency vs. inverse area.

This leads to (11) where the oxide thickness (T_{OX}) is included in order to provide some degree of technology independence. Note that $f_{PEAK\text{-}Q}$ should be inserted in GHz.

$$A_{INDUCTOR} \approx \frac{18000\mu m \cdot T_{OX}}{f_{PEAK-Q}} \qquad (11)$$

The innermost inductor turns do not contribute positively to the quality of the inductor. Therefore the inner diameter should be large. On the other hand a too large inner diameter would reduce the inductance (due to the smaller number of inductor turns) therefore this is not desired either. Five inductors were integrated in order to investigate what the optimum inner diameter is. They are based on an inductor with, S=2μm, W=6μm and 10 turns filled up to the center. Each inductor has one turn more taken away than the next. This gives inner diameters of 8, 24, 40, 56 and 72μm. As with figure 3, a contour plot was generated (figure 6). It shows an optimum Q-value (4.6) above an inner diameter of 56μm. The peak is found somewhere near 64μm but as the peak-Q frequency is increasing along with the inner diameter (due to the smaller area) the Q-value could be improved by slightly increasing the wire width. This means that the optimum is probably found at a slightly higher diameter. We believe that the optimum is near a 70-90μm diameter for a 5 nH inductor.

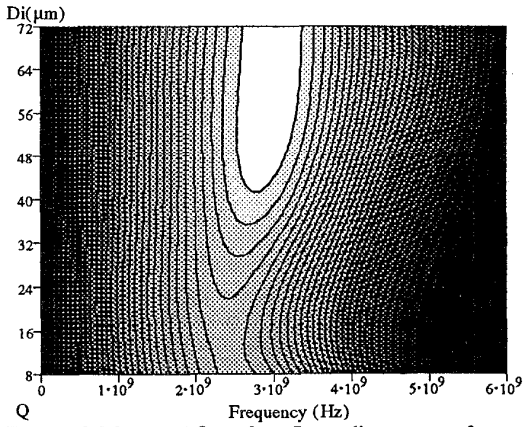

Figure 6. Measured Q-surface. Inner diameter vs. freq.

5. DESIGN GUIDE TO ON-CHIP CMOS INDUCTORS

This design guide is based on the results found in the analysis of the test inductors and the results presented in resent papers. It covers all issues involved with the design of good one-layer on-chip inductors in CMOS processes.

1) Process. If it is possible, a process should be chosen with A) Low metal resistivity in the upper metal layers. B) As many metal layers as possible. C) Large oxide thickness (between substrate and metal layers). D) High substrate resistivity (a typical submicron CMOS process has a substrate resistivity of 0.01 Ω·cm).

2) Peak-Q frequency. For most applications it is advantageous that the inductor has a peak-Q (defined as (10)) at the frequency of operation. If a large inductance value is desired the peak-Q frequency may be chosen perhaps 10-15% lower than the frequency of operation because the Q-value changes little in the proximity of the peak-Q frequency and because this will give the possibility of using a larger inductor. The exception is the case where the inductor is used in an LC-tank e.g. in an LC-oscillator. In this case the peak-Q frequency can be chosen considerably smaller than the frequency of operation because some of the parasitic inductor capacitance can be used in the LC-tank. The self-resonance frequency, on the other hand, must still be well above the frequency of operation. A reasonable compromise is to choose the peak-Q frequency 30-40% below the frequency of operation.

3) Layer topology. Metal1 should not be used for inductor turns - *it is simply too close to the substrate. In a two metal-layer* process Metal2 must be used for the inductor turns. In a three metal-layer process Metal3 is used for the inductor turns. Metal2 may also be used in a stacked configuration (coupled in shunt) if the relative improvement in conductivity is greater than the increase in capacitive coupling to the substrate. The same scheme applies for processes with more metal layers.

4) Inductor area. There is a close interrelation between inductor area and the Peak-Q frequency so an area should be estimated that with the chosen layer topology give approximately the peak-Q frequency decided on. In order to do so, use (11) to calculate the area that gives the desired peak-Q frequency. Note that this area includes wire spacing and fringing fields.

5) Inductor shape. The shape that has the shortest perimeter for a given area is the circle. Therefore an inductor with circular turns has the highest number of turns for a given wire length and center-area. This means that the circular inductor gives the highest inductance value and hence the highest Q-value (other parameters are not affected by the shape). An octagonal shape has a 2.7% longer perimeter and a square has a 12.8% longer perimeter than the circle. This means that octal inductor can be used with a minimal penalty. A square inductor can be used if the Q-value is of minor importance.

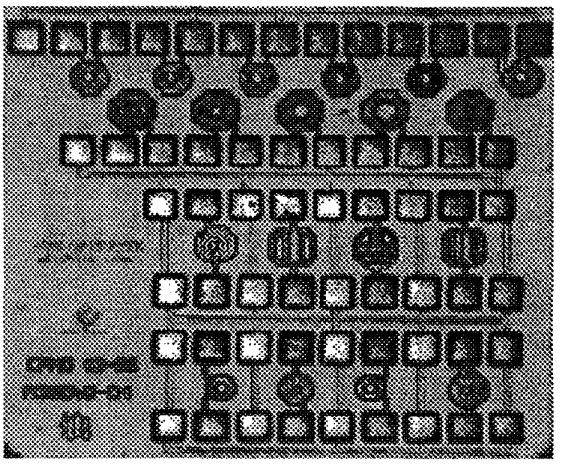

Figure 7. Microphotograph of one of the test chips.

6) Center hole. Inductor turns close to the center have a negative effect on the quality of the inductor. Therefore a large hole should be made in the center of the inductor. The measurements indicate that for a 5.0 nH inductor a center hole with an average radius (to the edge of the innermost turn) of 35-45μm give optimal conditions. It is reasonable to assume that a larger inductor should have a slightly bigger hole due to the stronger field.

7) Average outer radius. The inductor area and average inner radius have been chosen. This means that the average outer radius can be calculated. It is given by (12) where W_{FRI} is the equivalent width of the fringing field (typically $W_{FRI} \approx 3.5\mu m$).

$$R_O \approx \sqrt{(R_I - W_{FRI})^2 + \frac{A_{IND}}{\pi}} - W_{FRI} \qquad (12)$$

8) Inductance, number of turns. Good inductors in CMOS processes have wire widths of approximately 7-20μm where the small widths give large inductance values with reasonable Q-factor and the large widths give higher Q-values and much smaller inductance. For a large inductance a W of 7-9μm is a good compromise. For a high Q-value (though not much higher) a reasonable compromise would be a W of 14-18μm. This give a range of inductance values that are feasible for a given process and a given application. To find the maximum inductance use (1) and (2) with W=7μm and S=2μm to calculate a rough estimate of L_max. Use W=20μm and S=2μm to calculate a rough estimate of L_min. Q-values of 6.0-5.0 can be expected for a small inductance and 5.5-4.5 can be expected for a large inductance in an average submicron CMOS process. Choose an inductance value and calculate W+S using (1) and (2).

9) Wire width and spacing. For a 3.3nH inductor with 6 turns and W+S =8μm the optimal spacing was found to be 1.9μm. For wire widths that are larger, the relative penalty in resistance of increasing the spacing is smaller so the optimum spacing would be slightly higher. Therefore add a few tenths of microns for higher W. If more layers are used for the turns the capacitive

coupling between the turns increases. Therefore for two or more layers add a couple of tenths of microns to the spacing. In other words use a spacing of 2.0-2.1 μm for a one-layer inductor with W=9μm and use a spacing of 2.2-2.4 μm for a two-layer inductor with W=9μm. As we found W+S before we now have both the wire spacing and width. Thereby all design parameters have been found.

10) Simulation. The designer may now want to simulate the performance of the inductor in a model of the intended application to verify that this is really the appropriate inductor. The model described in section 3 can be used for the simulation.

11) Inductor layout. If the inductor is the desired one, the lay out can be made. In doing so a couple of good design practices should be followed. As low series resistance is of utmost importance be sure to connect the inside of the inductor to the outside with a bridge with sufficiently low resistance. Use (a) lower laying metal layer(s) with a width that give a resistance per length not too far from the one used for the turns. 10-15μm is acceptable. Further be sure to use enough vias. The resulting via resistance should be in the order of the sheet resistance. Usually 20-30 vias is enough. At the outside of the inductor bring the connecting bridge back up into the same layers as used for the turns. Slightly wider metal may be used for the connecting strips. Finally make sure an area surrounding the inductor is cleared to ensure that the inductor does not interact with neighboring circuitry. The inner radius can be used as a measure of a reasonable distance to surrounding circuitry/metal.

12) Test layout considerations. For test purposes use the pad configuration specified by the probe station. Further place them far from the inductor (70-100μm or more) and use plenty of substrate contacts as the pads seriously contaminate the substrate (at GHz frequencies) and thereby the inductor measurements. Further make an identical layout (with substrate contacts, identical proximities and everything) but without the inductor itself. This way the parasitics of the pads can be measured and de-embedded from the inductor measurements.

6. MULTI LAYER INDUCTORS

A number of inductors were fabricated in order to investigate the properties of multi-layer inductors. Some were coupled in a stacked configuration to reduce the series resistance and others had inductor turns in both metal2 and metal3 to increase the inductance value. The inductors turned out to be almost as good as the single layer metal3 inductors. The reason why they did not turn out to be better than the single layer inductors was that the increased capacitance and the poor conductivity of the metal2 layer (60 mΩ/sq. compared to 38mΩ/sq. in the metal3 layer) degraded performance substantially.

Multi-layer inductors may not be very interesting in average two or three-metal layer processes but in state-of-the-art CMOS processes and in future processes they may be very interesting especially as the trend goes towards having low resistivity metal4 and metal5 layers. Therefore further investigation in the design of multi-layer inductors is important.

7. CONCLUSION

This paper has presented an easy and straightforward method of modeling on-chip CMOS inductors through the use of a lumped element model and a number of new empirical and semi-empirical formulas. This enables easy simulation in SPICE-like simulators. A number of test results based on measurements have been presented concerning optimal metal spacing, size of center hole, self-inductance and inductor area. We found that the optimal metal spacing is close to 2.0 μm and that the optimal inner radius is 35μm-45μm for a 5nH inductor. Finally a comprehensive design guide has been presented that shows how close-to-optimal inductors can be designed with a minimal effort.

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